STANDARD TEMPLATE OF FACULTY PROFILE FOR UPLOADING OF UNIVERSITY WEBSITE

Title	DR.	First Name	VANDANA	Last Name	NATH	
Designation		ASSOCIATE PROFESSOR				
School /Dept. Name		USIC&T				
Address:		E-212, E-BLOCK, GGSIPU, SEC-16C, DWARKA, DELHI-110078				
Phone No.		Office	011-25302734			
		Residence	(optional)			
		Mobile	(optional)			
Email		1. vandana.nath@ipu.ac.in		2.vandanausit@gmail.com		
Web Page (if any)						
Subjects Taught		• Electronics Devices & Circuits • Analog Electronics • Linear Integrated Circuits • Optical Fiber Communication • Transmission Lines, waveguides and Antenna • Information Theory & Coding • Microwave Integrated Circuits • MEMS & Sensor Technology • Electrical Science				
Areas of Interest/ Specialization		Modelling of HEMT/MOSFET Devices, Optical Fiber Communications, Antenna, Microwave Engg.				
Experience (in years)		Total	21 years			
		Industry	Nil			
		Teaching	16 years			
		Research	5 years			
Educational Qualifications		UG	B.Sc. (PCM)			
		PG	M.Sc. (Electronics), M.Tech (ECE)			
		Doctorate	Ph.D. (Electronics Science)			
		Any other – Diploma in IPR	-			

Research Publications in Journals (last 5 years)	1 "Enhanced Analog Performance and High-Frequency Applications of Dielectric Engineered High-K Schottky Nanowire FET" Swati Sharma, Anubha Goel, Sonam Rewari, Vandana Nath, RS Gupta, Silicon, Feb 2022, https://doi.org/10.1007/s12633-022-01663-1 2 "Dual-band Elliptical Wide-Slot Antenna with High BDR for Portable Wireless Applications", M. Kumar and V. Nath, International Journal of Electronics, Sept. 2020. [DOI: 10.1080/00207217.2020.1818295] [ISSN: 1362-3060] 3 "A Circularly Polarized Printed Elliptical Wide Slot Antenna with High Bandwidth-Dimension-Ratio for Wireless Applications," M. Kumar and V. Nath, Wireless Networks, vol. 26, pp. 5485-5499, June 2020. (SCI, Impact Factor-2.659) [DOI: 10.1007/s11276-020-02399-9] [ISSN: 1022-0038] 4 "Design and Development of Triple-band Compact ACS-fed MIMO Antenna for 2.4/3.5/5 GHz WLAN/WiMAX Applications," M. Kumar and V. Nath, Analog Integrated Circuits and Signal Processing, vol. 103, pp. 461-470, Mar. 2020. [DOI: 10.1007/s10470-020-01626-9] [ISSN: 0925-1030] 5 "A High BDR Microstrip-line-fed Antenna with Multiple Asymmetric Elliptical Wide-slots for Wideband Applications," M. Kumar and V. Nath, International Journal of RF and Microwave Computer-Aided Engineering, vol. 30, no. 7, pp. e22202, Feb. 2020. [DOI: 10.1002/mmce.22202] [ISSN: 1096-4290] 6 Circularly Polarized Microstrip-Line-Fed Antenna with Rotated Elliptical Slot Serving Satellite Communications", Munish Kumar, Vandana Nath, Wireless Personal Communications, Volume 110, Issue 3, pp 1443–1458, 2020 7 "A compact flower-shaped printed monopole MIMO antenna for wideband applications", V Nath, M Kumar, Radio Science, Volume 54, Issue 11, Pages 963-974, Nov 2019 8 "Dual metal Schottky barrier asymmetric gate stack cylindrical gate all around (DM-SB-ASMGS-CGAA) MOSFET for improved analog performance for high frequency application" Shreya Nandy, Sanjana Srivastava, Sonam Rewari, Vandana Nath, R. S. Gupta, Microsystem Technologies, Aug 2019, pg.1-10 https://doi.org/10.1007/s00542-019-04577-y 9 "Novel design to improve band to band tunneling and gate induced drain leakages (GIDL) in cylindrical gate all around (GAA) MOSFET", Sonam Rewari, Vandana Nath, Subhasis Haldar, SS De swal, RS Gupta, Microsystem Technologies, Vol. 25, No. 5, pg.1537-1546, 2019 10 "Hafnium oxide based cylindrical junctionless double surrounding gate (CJLDSG) MOSFET for high speed, high frequency digital and analog applications", Sonam Rewari, Vandana Nath, Subhasis Haldar, SS Deswal, RS Gupta, Microsystem Technologies, Vol. 25, No. 5, pg. 1527-1536, 2019 11 "Microstrip-Line-Fed Elliptical Wide-slot Antenna with Similar Parasitic Patch for Multiband Applications", Munish Kumar, Vandana Nath, IET Microwaves, Antennas & Propagation, Vol.12, Issue 14, pg. 2172-2178, Nov 2018, DOI: 10.1049/iet-map.2018.5377 , Print ISSN 1751-8725, Online ISSN 1751-8733 12 "Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET" Sonam Rewari, Vandana Nath, Subhasis Haldar, SS Deswal, RS Gupta, IEEE Transactions on Electron Devices 65 (1) 2018

	13 "Introducing multiband and wideband microstrip patch antennas using fractal geometries: Development in last decade", Munish Kumar, Vandana Nath, Wireless Personal Communications, 98 (2) 2018 14 "Improved analog and AC performance with increased noise immunity using nanotube junctionless field effect transistor (NJFET)" Sonam Rewari, Vandana Nath", Subhasis Haldar, S. S. Deswal, R. S. Gupta, Applied Physics A, Vol. 122, no. 12, Pages 1049, 2016 15 "Numerical modeling of Subthreshold region of junctionless double surrounding gate MOSFET (JLDSG)", Sonam Rewari, Subhasis Haldar, Vandana Nath, S.S. Deswal, R.S. Gupta, Superlattices and Microstructures, Volume- 90, Pages 8-19, 2016
Papers Published in Conference Proceedings(last 5 years)	1. *"Impact of Reverse Gate Oxide Stacking on Gate All Around Tunnel FET for High Frequency Analog and RF Applications",* A Das, BK Kanaujia, V Nath, S Rewari, RS Gupta, 2020 IEEE 17th India Council International Conference (INDICON) 10-13 Dec. 2020, New Delhi, India **DOI:** 10.1109/INDICON49873.2020.9342175 2. *"Schottky Barrier Double Surrounding Gate MOSFET for High-Frequency Implementation",* Swati Sharma; Sonam Rewari; Vandana Nath; S.S. Deswal; R. S. Gupta, 2020 5th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE), 1-3 Dec. 2020 **DOI:** 10.1109/ICRAIE51050.2020.9358359 3. "*Comparison of Linearity and Intermodulation Distortion Metrics for T-and Pi-Gate HEMT*", Khushwant Sehra, Vandana Kumari, Vandana Nath, Mridula Gupta, DS Rawal, Manoj Saxena, 2019 International Conference on Electrical, Electronics and Computer Engineering (UPCON), 8-10 Nov. 2019, **DOI:** 10.1109/UPCON47278.2019.8980221 4. *"Optimization of Asymmetric π Gate HEMT for Improved Reliability & Frequency Applications"* Khushwant Sehra, Vandana Kumari, Vandana Nath, Mridula Gupta, Manoj Saxena, IEEE 9th International Nanoelectronics Conferences (INEC) July 2019, **DOI:** 10.1109/INEC.2019.8853857 5. *Open Ended Microstrip-line-fed Compact Wideband MIMO-Diversity Antenna with Multiple Asymmetric Elliptical Wide-Slots,* M Kumar, V Nath, 2019 URSI Asia-Pacific Radio Science Conference (AP-RASC), **DOI:** 10.23919/URSIAP-RASC.2019.8738508 6. *Dual-Band Dual-Polarized Stacked Octagonal Fractal Patch Antenna with Nonlinear Manipulation,* Munish Kumar ; Vandana Nath, 2018 IEEE Radio and Antenna Days of the Indian Ocean (RADIO), 15-18 Oct. 2018, **DOI:** 10.23919/RADIO.2018.8572374 7. *Triple Band Non-Linear Manipulated Sierpinski-Knopp Fractal Wide-Slot Microstrip Antenna with Inverted L-shaped Strip,* Ankit Chand, Munish Kumar, Vandana Nath, 2nd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), Kolkata, India, 4-5 May 2018 **DOI:** 10.1109/IEMENTECH.2018.8465193 8. *"Multiband CPW-fed Circular Microstrip Antenna with Modified Cantor Fractal Slot for DCS/GPS/WiMAX/WLAN/HiPERLAN2 Applications",* Munish Kumar ; Vandana Nath, 2018 International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET), 22-24 March 2018 **DOI:** 10.1109/WiSPNET.2018.8538537

<table>
<tr><td></td><td colspan="4">
9. *"Improved cross polarization and wideband multilayer wide-slot microstrip antenna with rotated parasitic patch",* Munish Kumar, Vandana Nath IEEE Asia Pacific Microwave Conference (APMC), 2017, 964-967
10. *"Dual metal (DM) Insulated Shallow Extension (ISE) Gate All Around (GAA) MOSFET to reduce gate induced drain leakages (GIDL) for improved analog performance"* Sonam Rewari, Vandana Nath, Subhasis Haldar, SS Deswal, RS Gupta, IEEE Devices for Integrated Circuit (DevIC), Kalyani, India, 23-24 March 2017, 401-406 **DOI:** 10.1109/DEVIC.2017.8073979
11. *"A numerical model of GaN based cylindrical junctionless gate all around MOSFET for subthreshold region at cryogenic temperatures"*, Sonam Rewari, Vandana Nath, Subhasis Haldar, SS Deswal, RS Gupta, IEEE Devices for Integrated Circuit (DevIC), Kalyani, India, 23-24 March 2017, 422-427 **DOI:** 10.1109/DEVIC.2017.8073984
12. *"GaN based Junctionless Double Surrounding Gate (JLDSG) MOSFET for high power, high voltage and high frequency applications"* Sonam Rewari, Vandana Nath, Subhasis Haldar, SS Deswal, RS Gupta, Asia-Pacific Microwave Conference (APMC), New Delhi, India, 5-9 Dec. 2016, 1-4 **DOI:** 10.1109/APMC.2016.7931265
13. *"Dual-band microstrip line-fed antenna with fractal Spidron defected ground structure*", Munish Kumar, Vandana Nath, IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), 24-27 Oct. 2016, Phuket, Thailand, 1-6. **DOI:** 10.1109/ISPACS.2016.7824700
14. *"Design and simulation of tri-band spidron fractal equilateral triangle microstrip antenna"* Munish Kumar, Vandana Nath, IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI), 21-24 Sept. 2016, 287-293
15. *"AC analysis of Junctionless Double Surrounding Gate (JLDSG) MOSFET for Tera Hertz applications"* IEEE International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), New Delhi, India, 11-13 March 2016, 113-117
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<tr><td>Books Authored/ BookVolume Chapters</td><td colspan="4"></td></tr>
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<tr><td colspan="2">-</td><td>-</td></tr>
<tr><td>International</td><td colspan="2">3</td><td>1</td></tr>
<tr><td rowspan="3">Research Guidance</td><td rowspan="2">Awarded</td><td>PG</td><td>M. Phil</td><td>Doctorate</td></tr>
<tr><td>30 (Approx.)</td><td>NA</td><td>02</td></tr>
<tr><td>Undergoing</td><td>02</td><td>NA</td><td>04</td></tr>
<tr><td rowspan="2">Research Projects</td><td>Completed</td><td colspan="3">Project titled "Design and Optimisation of fractal based microstrip antenna for bandwidth enhancement and multiband functionality" of 1.8Lakh funded by GGSIPU under Faculty Research Grant Commission in 2017-2018</td></tr>
<tr><td>Undergoing</td><td colspan="3">Nil</td></tr>
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Awards & Distinctions	1. Senior Research Fellowship from DRDO, Solid State Physics Laboratory (SSPL), Delhi (2002-2004) 2. Junior Research Fellowship from DRDO, Solid State Physics Laboratory (SSPL), Delhi (1999-2001). 3. Gold Medal (2010), MTech (ECE)W, GGSIPU
Administrative Assignments Handled	1. Member, Board of Studies, 2017-2019 2. Convener/Member, SRC, USICT, 2013 onwards 3. Co-Ordinator, SRC-I, USET, 2013-14 4. Convenor, Academic Audit, 2013 to 2017 5. Admission Officer, MTech (ECE/VLSI) for sessions 2018-19 & 2021-2022 6. Convener, PhD Admission Committee ECE, 2013-2016 & 2017-2019 7. Convener, Syllabus Revision committee, PhD Programme, USICT, 2019 8. Co-Ordinator, M. Tech (ECE)Regular, 2017 to 2020 9. Co-Ordinator, Time Table committee, 2017-2020 10. In-charge/Convenor, Electronics System Lab 2010-till date 11. Member, Ordinance Revision Committee, GGSIPU, 2013-2014 12. Member, Compliance Report & Mandatory Discloser Committee, GGSIPU, 2009-2011 13. Member, Coordination Committee, Indraprastha Center for Art & Culture, GGSIPU, 2014 14. Member, Core committee, Minor Exam USS, 2009-2012 15. Member, Anugoonj Committee (2011-2012) 16. Member, Grievance Redressal committee, USICT 17. Member, Committee for Safety of Women and Gender Sensitization, USIC&T 18. Member, Vision Document 2030, USIC&T 19. Member, Syllabus Revision committee, MTech(ECE) programme, USIC&T, 2019 20. Member, Syllabus Revision committee, BTech(ECE) programme, USIC&T, 2019 21. Member, Organizing committee, Alumni Meet 2017, USIC&T 22. Member, Organizing committee, ICCTICT-2016 23. Member, Time Table Committee 2009-2010 24. Member, End Term Practical Exam committee, 2009-2014 25. Member, ISO/NAAC Coordination Committee, 2009-2012 & 2022 26. Member, Library committee of USICT, 2022 27. Member, Purchase Committee, USICT, 2022
Association with Professional Bodies	• Member IEEE • Life Member – Semiconductor Society of India (SSI) • Life Member – The Indian Society for Technical Education (ISTE)
Any other Achievements	1. External panel expert in two SRCs of DTU 2. Special Session Chaired in 11th IEEE International Conference IEEE RFID-TA 2021, Women Engineers in RFID