STANDARD TEMPLATE OF FACULTY PROFILE FOR UPLOADING OF UNIVERSITY WEBSITE

<table>
<tr><td>Title</td><td>Dr.</td><td>First Name</td><td>Manoj</td><td>Last Name</td><td>Kumar</td><td rowspan="3">  </td></tr>
<tr><td colspan="2">Designation</td><td colspan="4">Professor</td></tr>
<tr><td colspan="2">School /Dept. Name</td><td colspan="4">USIC&T</td></tr>
<tr><td colspan="2">Address:</td><td colspan="5">EFR-309, USIC&T, GGSIPU, Dwarka, New Delhi-110078</td></tr>
<tr><td colspan="2" rowspan="3">Phone No.</td><td>Office</td><td colspan="4">011-25302732</td></tr>
<tr><td>Residence</td><td colspan="4">(optional)</td></tr>
<tr><td>Mobile</td><td colspan="4">9873853870</td></tr>
<tr><td colspan="2">Email</td><td colspan="3">1. manojtaleja@ipu.ac.in</td><td colspan="2">2. manojtaleja@yahoo.com</td></tr>
<tr><td colspan="2">Web Page (if any)</td><td colspan="5">-</td></tr>
<tr><td colspan="2">Subjects Taught</td><td colspan="5">• Advanced VLSI Design
• VLSI Technology
• Analog Electronics
• Digital Electronics
• Low Power VLSI Design
• Microelectronics
• Electrical Science
• Circuits and System
• IC Design</td></tr>
<tr><td colspan="2">Areas of Interest/ Specialization</td><td colspan="5">• Microelectronics/VLSI Design</td></tr>
<tr><td colspan="2" rowspan="4">Experience (in years)</td><td>Total</td><td colspan="4">19.5</td></tr>
<tr><td>Industry</td><td colspan="4">-</td></tr>
<tr><td>Teaching</td><td colspan="4">19.5</td></tr>
<tr><td>Research</td><td colspan="4">-</td></tr>
<tr><td colspan="2" rowspan="4">Educational Qualifications</td><td>UG</td><td colspan="4">B. Tech. (Electronics and Communication)</td></tr>
<tr><td>PG</td><td colspan="4">M. Tech. (Microelectronics)</td></tr>
<tr><td>Doctorate</td><td colspan="4">Ph.D. (Electronics and Communication)</td></tr>
<tr><td>Any other – Diploma in IPR</td><td colspan="4">-</td></tr>
</table>

Research Publications in Journals (last 5 years)	• Manoj Kumar, Dileep Dwivedi, "Design of Dual-Delay-Path Low-Power VCRO with I-MOS Varactor Tuning," IETE Journal of Research, Taylor and Francis, pp. 1-10, June 2021. • Anil Khatak, Manoj Kumar, Sanjeev Dhull, "A 1.67 pJ/Conversion-step 8-bit SAR-Flash ADC Architecture in 90-nm CMOS Technology," International Journal of Electronics and Telecommunication, vol 67, no 3, pp. 437-354, 2021. • Manoj Kumar, "A Low Power Digitally Controlled Ring Oscillator Design with IMOS Varactor Tuning Concept," Journal of The Institution of Engineers (India): Series B, Springer, June 2021. • Dileep Dwivedi, Manoj Kumar and Vandana Niranjan, "Design of Power-Efficient CMOS Based Oscillator Circuit with Varactor Tuning Control," SN Applied Sciences, Springer, vol. 3, 487, March 2021. • Nitin Kumar and Manoj Kumar, "Low Power CMOS Differential Ring VCO Designs using Dual Delay Stages in 0.13 µm Technology for Wireless Applications," Microelectronics Journal, Elsevier, vol. 111, May 2021. • Vikram Singh, Sandeep Kumar Arya, and Manoj Kumar, "A Common‐Gate Current‐Reuse UWB LNA for Wireless Applications in 90 nm CMOS," Wireless Personal Communications, Springer, Feb 2021. doi: https://doi.org/10.1007/s11277-021-08287-5. • Nitin Kumar and Manoj Kumar, "Low Power wide Tuning Range Differential Ring VCO Designs with I-MOS and A-MOS Varactor," International Journal of Electronics and Communications (AEU), Elsevier, vol. 131, March 2021, 153583. ISSN: 16180399, 14348411. • Dinesh Kumar and Manoj Kumar, "Adiabatic Logic-based Strong ARM Comparator for Ultra-Low Power applications," Microsystems Technologies, Springer, ISSN: 0946-7076 (print), 1432-1858. • Nisha Chugh, Manoj Kumar Subhasis Haldar, Monika Bhattacharya & R.S. Gupta "Applicability of Field Plate in Double Channel GaN HEMT for Radio-Frequency and Power-Electronic Applications", Silicon, Springer, Electronic ISSN: 1876-9918, Print ISSN:1876-990X • Vivek Jangra and Manoj Kumar, "New low power differential VCO circuit designs with active load and IMOS varactor," International Journal of Electronics and Communications (AEU), Elsevier, pp. 153191, vol. 119, May 2020.

	• Vivek Jangra and Manoj Kumar, "Low power active load and IMOS varactor based VCO designs using differential delay stages in 0.18µm technology," Microelectronics Journal, Elsevier, vol. 98, pp. 104728, April 2020. ISSN: 09598324. • Dinesh Kumar and Manoj Kumar, "VLSI implementation of wave shaping diode based adiabatic logic (WSDAL)," International Journal of Electronics, Taylor and Francis, pp. 1-18, July, 2020, Print ISSN: 0020-7217, Online ISSN: 1362-3060. • Dinesh Kumar and Manoj Kumar, "Implementation of parallel computing and adiabatic logic in full adder design for ultra-low power applications," SN Applied Sciences, Springer, vol. 2, no. 8, pp. 1-11, July, 2020. ISSN 2523-3971. • Nisha Chugh, Manoj Kumar, M. Bhattacharya and R.S. Gupta, "Extraction and evaluation of admittance parameters of symmetrically doped AlGaN/GaN/AlGaN DH-MODFET-A comparison with SH-MODFET," Microsystems Technologies, Springer, pp. 1-8, Feb. 2020. ISSN: 0946-7076 (print). • Dinesh Kumar and Manoj Kumar, "Signal aware energy efficient approach for low power full adder design with adiabatic logic", Microsystems Technologies, Springer, Nov 2020. https://doi.org/10.1007/s00542-020-05056-5. • Vivek Jangra and Manoj Kumar, "Low Power Single Ended VCO Design with IMOS Varactor for Wireless Applications," Telecommunications and Radio Engineering Journal, Begell House, vol. 79, issue 12, pp. 1073-1082, 2020. • Dileep Dwivedi and Manoj Kumar, "A 0.7-2.4 GHz Low Power VCO Design with Inversion MOS Varactor Tuning," Telecommunications and Radio Engineering Journal, Begell House, vol. 79, issue 3, pp. 249-260, 2020. • Shweta Dabas and Manoj Kumar, "A CMOS based low power digitally controlled oscillator design with MOS varactor," Analog Integrated Circuits and Signal Processing, Springer, vol. 100, issue 5, pp. 565-575, 2019. • Nitin Kumar and Manoj Kumar, "Low power ring VCO with pre-charge and pre-discharge circuit for 4 - 6.1 GHz applications in 0.18 µm CMOS," Journal of Circuits, Systems, and Computers, World Scientific Publishing,

	vol. 28, no. 21, 1950182, 2019. • Nisha Chugh, Manoj Kumar, Monika Bhattacharya, and R. S. Gupta. "Analysis of Al 0.15 Ga 0.85 N/GaN/Al 0.15 Ga 0.85 N DH-HEMT for RF and microwave frequency applications," Semiconductors, Springer, vol. 53, no. 13, pp. 1784-1791. 2019. • Vivek Jangra and Manoj Kumar, "A wide tuning range VCO design using multi-pass loop complementary current control with IMOS varactor for low power applications," International Journal of Engineering Science and Technology, Elsevier, vol. 22, issue 4, pp. 1077-1086, 2019. • Nisha Chugh; Manoj Kumar; Monika Bhattacharya; R.S. Gupta, "Sheet carrier concentration and current-voltage analysis of Al0.15Ga0.85N/GaN/Al0.15Ga0.85N double heterostructure HEMT incorporating the effect of traps," Microsystems Technologies, Springer, pp 1–10, 2019. • Dileep Dwivedi and Manoj Kumar, "Design of a 3-bit digital control oscillator (DCO) using IMOS varactor tuning," Analog Integrated Circuits & Signal Processing, Springer, vol.100, no. 3, pp. 613-620, 2019. • Vikram Singh, Sandeep Kumar Arya, and Manoj Kumar, "A 5.7 mW, UWB LNA for wireless applications using noise canceling technique in 90 nm CMOS," Frequenz Journal, De Gruyter Publisher, vol. 74, issue 1-2, pp. 83-93, 2019. ISSN, 21916349, 00161136. • Manoj Kumar, Vivek Jangra, "A low power VCO design using composite load for delay cell with IMOS varactor for wider tuning range," Journal of Information & Optimization Sciences, Taylor & Francis, vol. 40, issue 2, pp. 567-585, 2019. • Manoj Kumar, "Voltage controlled oscillator design using MOS varactor," Journal of The Institution of Engineers (India): Series B, Springer, vol. 100, issue 5, pp. 515-524, 2019. • Nitin Kumar and Manoj Kumar, "Design of CMOS based low power high frequency differential ring VCO," International Journal of Electronics Letter, Taylor & Francis, vol. 7, no.2, pp. 143-153, 2019. • Vivek Jangra, Manoj Kumar, "A minimum power VCO design using IMOS varactor for portable RF circuits," Journal of Engineering and Applied Science Research, vol. 46, no. 4, pp. 331-339, 2019. • Vikram Singh, Sandeep Kumar Arya, and Manoj Kumar, "A 3–14 GHz, self

	body biased common gate UWB LNA for wireless applications in 90nm CMOS," Journal of Circuits, Systems, and Computers, World Scientific Publishing, vol. 28, issue 4, 1950056, 2019. ISSN: 0218-1266 (print); 1793-6454 (web). • Manoj Kumar and Dileep Dwivedi, "Design of low power varactor based voltage controlled oscillator," International Journal of Information Technology, Springer, pp. 1-9, 2019. ISSN: 2511-2104. • Manoj Kumar "Design of linear low power voltage controlled oscillator with I-MOS varactor and back gate tuning," Circuits, Systems & Signal Processing (CSSP), Springer, vol. 37, issue 9, pp. 3685–3701, 2018. ISSN: 1531-5878. • Manoj Kumar and Dileep Dwivedi, "A low power CMOS based VCO design with I-MOS varactor tuning control," Journal of Circuits, Systems, and Computers, World Scientific Publishing, vol. 27, no. 10, 1850160, 2018. ISSN: 0218-1266 (print); 1793-6454 (web). • Vikram Singh, Sandeep Kumar Arya, and Manoj Kumar, "Gm-boosted current-reuse inductive-peaking common source LNA for 3.1 - 10.6 GHz UWB wireless applications in 32nm CMOS," Analog Integrated Circuits and Signal Processing, vol. 97, issue 2, pp 351–363, 2018. ISSN: 0925-1030 (Print) 1573-1979 (Online). • Nisha Chugh; Monika Bhattacharya; Manoj Kumar, R S Gupta, "Polarization dependent charge control model for microwave performance assessment of AlGaN/GaN/AlGaN double heterostructure HEMT," Journal of Computational Electronics, Springer, vol. 17, Issue 3, pp 1229–1240, 2018. • Vikram Singh, Sandeep Kumar Arya, and Manoj Kumar, "A 0.7 V, ultra-wideband common gate LNA with feedback body bias topology for wireless applications," Journal of Low Power Electronics and Applications, vol. 8, no. 42, pp.1-13, 2018. ISSN 2079-9268. • Anil Khatak, Manoj Kumar, Sanjeev Dhull "An improved CMOS design of Op-Amp comparator with gain boosting technique for data converter circuits," Journal of Low Power Electronics and Applications, vol. 8 no. 33, pp 1-16, 2018. ISSN 2079-9268. • Dinesh Kumar and Manoj Kumar, "Comparative analysis of adiabatic logic challenges for low power CMOS circuit designs," Microprocessors and Microsystems, Elsevier, vol. 60, pp. 107-121, 2018, ISSN: 0141-9331.

	• Prachi gupta, Manoj Kumar "Design of modified low power CMOS differential ring oscillator using sleepy transistor concept," Analog Integrated Circuits and Signal Processing. Springer, vol. 96, issue 1, pp. 87-104, 2018. ISSN: 0925-1030 (Print) 1573-1979 (Online). • Manoj Kumar, "CMOS oscillator with MOS varactor and body bias tuning," International Journal of Circuits and Architecture Design, Inderscience Publishers, vol. 2, issue 1, pp. 68-82, 2016. • Dileep Dwivedi and Manoj Kumar "Design of low power VCO based on single ended delay cells," International Journal of Circuits and Architecture Design, Inderscience Publishers, vol. 2, no.3-4, pp. 233-245, 2016. • Manoj Kumar, "VCO Design using NAND gate for low power application," Journal of Semiconductor Technology and Science, IEIE Korea, vol.16, no.5, pp.650-656, 2016. ISSN: 15981657. • Manoj Kumar, Sandeep K. Arya, and Sujata Pandey, "VCO design with variable capacitance XNOR delay cell," Journal of the Institution of Engineers (India): Series B, Springer, vol. 96, no. 4, pp. 371-379, 2014. • Manoj Kumar, "A Low Power voltage controlled oscillator design," ISRN Electronics, Hindwai Publishers, vol. 2013, article ID 987179, 6 pages, 2013. doi:10.1155/2013/987179. • Manoj Kumar, Sandeep K. Arya, and Sujata Pandey, "Low power digitally controlled oscillator designs with novel 3 transistors XNOR gate," Journal of Semiconductor, IOPscience Publishing, vol. 33, no.3, pp. 5001-8, March 2012. ISSN: 1674-4926. • Manoj Kumar, Sandeep K. Arya and Sujata Pandey, "Low power CMOS full adder design with body biasing approach," Journal of Integrated Circuits and Systems, Brazil, vol. 6, no.1, pp.75-80, 2011. ISSN 1807-1953. • Manoj Kumar, Sandeep K. Arya, Sujata Pandey, "digitally controlled oscillator design with variable capacitance XOR gate," Journal of Semiconductor, IOPscience Publishing, vol. 32, no. 10, pp. 105001-7, 2011.
Papers Published in Conference Proceedings(last 5 years)	• Vivek Jangra and Manoj Kumar "Low Power XNOR based Single Ended VCO Cir-cuit Design with Dynamic Threshold MOS" In 2021 Thirteenth International Conference on Contemporary Computing (IC3-2021) (IC3 '21), August 5–7, 2021, Noida, India. ACM, New York, NY, USA), (https://doi.org/10.1145/3474124.3474141)

	• Dileep Dwivedi and Manoj Kumar, “An Improved CMOS Ring VCO Design with Resistive-Capacitive Tuning Method” International Conference on Paradigms of Communication, Computing and Data Sciences (PCCDS 2021). NIT Kurukshetra, India, pp. 39-48, March 2021. • Dileep Dwivedi and Manoj Kumar “A Low-Power Ring Voltage-Controlled Oscillator with MOS Resistor Tuning for Wireless Application,” Proceedings of International Conference on Artificial Intelligence and Applications, vol. 1164, pp. 163-171, Springer, Singapore, 2020. Print ISBN: 978-981-15-4991-5. https://doi.org/10.1007/978-981-15-4992-2-16. • Sameer Kumar Jha ; Parv Verma; Manoj Taleja, “Design of Low Power CMOS Based Schmitt Trigger in 180nm Technology,” 2019 4th IEEE International Conference on Internet of Things: Smart Innovation and Usages (IoT-SIU), Ghaziabad, India, India, 18-19 April 2019, pp. 1-5. DOI: 10.1109/IoT-SIU.2019.8777506. Electronic ISBN: 978-1-7281-1253-4,CD: 978-1-7281-1252-7. • A. Bhardwaj, V. Chauhan and M. Kumar, "Design of CMOS based D flip-flop with different low power techniques," 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India, 7-8 March 2019, pp. 834-839. doi: 10.1109/SPIN.2019.8711610. Electronic ISBN: 978-1-7281-1380-7,CD: 978-1-7281-1379-1 • D. Tailor, T. Sharma and M. Kumar, "Design of CMOS based 1-bit comparator with MTCMOS and forced stack technique in 180nm technology," 2019 4th International Conference on Internet of Things: Smart Innovation and Usages (IoT-SIU), Ghaziabad, India, 18-19 April 2019, pp. 1-7. doi: 10.1109/IoT-SIU.2019.8777496. Electronic ISBN: 978-1-7281-1253-4, CD: 978-1-7281-1252-7. • Manoj Kumar, "Design of voltage controlled oscillator with resistive and IMOS varactor tuning," 2018 4th International Conference on Computing Communication and Automation (ICCCA), Greater Noida, India, 2018, pp. 1-4. • Nisha Chugh, Manoj Kumar, M. Bhattacharya and R. S. Gupta, "RF performance comparison of dual material gate (DMG) and conventional AlGaN/GaN high electron mobility transistor," 2018 4th International

	Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, March 2018, pp. 137-142. • Manoj Kumar, "Design of low power voltage controlled oscillator with RC delay element tuning," IEEE International conference on computing for sustainable global development INDIACom-2018, Bharati Vidyapeeth, New Delhi,14th - 16th March, 2018, pp. 493-496. ISSN 0973-7529; ISBN 978-93-80544-28-1. • Dinesh Kumar and Manoj Kumar "Design of low power full adder using two-phase clocked adiabatic static CMOS logic," Proceedings of First International Conference on Smart System, Innovations and Computing. Smart Innovation, Systems and Technologies, vol 79. Springer, Singapore Manipal University, Rajasthan, 2018. DOI:https://doi.org/10.1007/978-981-10-5828-8-53, ISBN: 978-981-10-5828-8. • Nisha Chugh, Monika Bhattacharya, Manoj Kumar and R.S Gupta, " Impact of donor-layer doping & thickness, gate-length and temperature on potential and electron concentration in AlGaN/GaN Double-Heterostructure and Single-Heterostructure HEMT," 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON-2018), Nov. 2018, pp. 1-5. • Vikram Singh, Sandeep Arya and Manoj Kumar, "Effect of resistive feedback on performance parameters of common source LNA," 2017 International Conference on Computing, Communication and Automation (ICCCA), Greater Noida, 2017, pp. 298-303. doi: 10.1109/CCAA.2017.8229819. • P. Gupta and M. Kumar, "Power efficient voltage controlled oscillator design in 180nm CMOS technology," 2017 International Conference on Computing, Communication and Automation (ICCCA), Greater Noida, 2017, pp. 1470-1476. doi: 10.1109/CCAA.2017.8230032 2017, Galgotia University. • N. Chugh, M. Bhattacharya, M. Kumar and R. S. Gupta, "Sheet carrier concentration and threshold voltage modeling of asymmetrically doped AlGaN/GaN/AlGaN double heterostructure HEMT," 2017 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), Mathura, 2017, pp. 446-451. doi:

	10.1109/UPCON.2017.8251089. • N. Kumar and M. Kumar, "Design of low power and high speed phase detector," 2016 2nd International Conference on Contemporary Computing and Informatics (IC3I), Noida, India, 14 - 17 Dec 2016, pp. 676-680. doi: 10.1109/IC3I.2016.7918048. • D. Kumar and M. Kumar, "Design of low power two bit magnitude comparator using adiabatic logic," 2016 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), Phuket, Thailand, 2016, pp. 1-6. • S. Dabas and M. Kumar, "A new design of digitally controlled oscillator for low power applications," 2016 2nd International Conference on Contemporary Computing and Informatics (IC3I), Noida, 14 - 17 Dec 2016, pp. 671-675. doi: 10.1109/IC3I.2016.7918047 . • D. Kumar and M. Kumar, "Modified 4-2 compressor using improved multiplexer for low power applications," 2016 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Jaipur, 2016, pp. 236-242.
Books Authored/ BookVolume Chapters	• Dinesh Kumar and Manoj Kumar, "Adiabatic logic based full adder design with leakage reduction mechanisms," in International Conference on Signal Processing and Communication, Book series Advances in Signal Processing and Communication, vol. 526, pp. 511-520, 2019. • Nitin Kumar and Manoj Kumar, "Design of low power and high speed CMOS phase frequency detector for a PLL," in International Conference on Signal Processing and Communication, Book series Advances in Signal Processing and Communication, 2019, vol. 526, pp. 529-540. • A. Khatak, M. Kumar and S. Dhull "Design and analysis of a 4-bit flash ADC architecture with modified comparator," International Conference on Intelligent Data Communication Technologies and Internet of Things (ICICI) 2018. Lecture Notes on Data Engineering and Communications Technologies,

<table>
<tr><td></td><td colspan="4">vol 26, 2018. Springer.

• Manoj Kumar, Sujata Pandey and Sandeep K. Arya, “Design of CMOS energy efficient single bit full adder,” International Conference on high performance and Grid Computing (Book chapter of communications in computer and information science, Springer-Verlag Berlin Heidelberg), Chitkara University, Rajpura, Punjab, CCIS 169, 2011, pp. 159-168. ISBN: 978-3-642-22576-5, D.O.I: 10.1007/978-3-642-22577-2-23.</td></tr>
<tr><td rowspan="3">No. of Conferences</td><td rowspan="2">National</td><td colspan="2">Attended</td><td>Organized</td></tr>
<tr><td colspan="2">-</td><td>-</td></tr>
<tr><td>International</td><td colspan="2">06</td><td>01</td></tr>
<tr><td rowspan="3">Research Guidance</td><td rowspan="2">Awarded</td><td>PG</td><td>M. Phil</td><td>Doctorate</td></tr>
<tr><td>50</td><td></td><td>05</td></tr>
<tr><td>Undergoing</td><td>02</td><td></td><td>04</td></tr>
<tr><td rowspan="2">Research Projects</td><td>Completed</td><td colspan="3">“Investigation and Design of High frequency, Low Power CMOS based Oscillator Circuits” Under Young Faculty Research Fellowship (2019-2021) of Visvesvaraya PhD Scheme for Electronics & IT, Ministry of Electronics & Information Technology, MeitY, Government of India</td></tr>
<tr><td>Undergoing</td><td colspan="3">-</td></tr>
<tr><td>Awards & Distinctions</td><td colspan="4">Awarded with Faculty Achievement Award for the Year 2019 in Guru Gobind Singh Indraprastha University, Dwarka, New Delhi, India</td></tr>
<tr><td>Administrative Assignments Handled</td><td colspan="4">• Coordinator M. Tech. Weekend (CSE/ECE) Program GGSIPU, Dwarka from Aug. 2020 to till date.
• Additional Coordinator M. Tech. Weekend (IT/CSE/ECE) Program GGSIPU, Dwarka from June 2017 to Aug. 2020.
• Coordinator B. Tech. (ECE) Program in USICT, GGSIPU, Dwarka from Jan. 2018 to till date.
• Coordinator B. Tech. and M. Tech. ECE Program in USICT, GGSIPU, Dwarka from Dec. 2013 to Sept. 2014.
• Member University Committee of Internal Quality Assurance Cell.
• Member of University core committee for NAAC and NIRF Accreditation.
• In charge of NIRF for year 2018, 2019 and 2020 for USICT.
• Member of Coordination Team for Inter College B. Tech. Major Project Competition 2016 and 2017, 2018, 2019.
• Centre Superintendent Conduct Examination for University Dec. 2018, May 2019, Dec. 2019 and March 2020.</td></tr>
</table>

	• Centre Superintendent Evaluation Centre for University Dec. 2014, May 2015, Dec. 2015, May 2016, Dec 2016 and May 2017. • Deputy Centre Superintendent Evaluation Centre for University Dec 2013 and May 2014. • Convener Academic audit USICT, GGSIPU 2017-18 and 2018-19. • Expert for Academic audit of USS, GGSIPU 2017-18 and 2018-19. • Member of Quality Improvement Cell, USICT from Oct. 2014 to till date. • Member Purchase Committee, USICT, 2014 onwards. • Members of various Committees related to UITS Cell, GGSIPU. • Member Admission Committee, International Affairs Admission 2015, 2016, 2017, 2018, 2019 and 2020. • Admission Officer M. Tech. Weekend Courses 2018 and 2019. • Expert for Grievance Redressal System for University Examinations 2014, 2015, 2016, 2017, 2018, 2019. • In charge Minor Examination Committee, USICT, GGSIPU from year 2014 to 2017. • Admission Officer (2014, 2015 and 2016, 2020) M Tech (CET Code-140) Admission Committee. • Convener/Expert Joint Assessment Committee 2015, 2016, 2017, 2018. • Expert Academic Audit Committee, GGSIPU, 2016, 2017 • Program Co-Chairs- ICCTICT 2016, GGSIPU, Dwarka, New Delhi.
Association with Professional Bodies	• Fellow, IE, India. • Life member of Indian society of Technical Education. • Life members of Institution of Electronics & Telecommunication Engineers. • Life member of Computer Society of India, Mumbai. • Life member of Semiconductor Society of India, New Delhi.
Any other Achievements	-